IN THE UNITED STATES PATENT AND

In re Patent Application of

GEVORGIAN ET AL. Atty. Ref.: 3670-66

TC/A.U.: Unknown Serial No. Unknown

Filed: June 6, 2006 Examiner: Unknown

For: A DELAY LOCKED LOOP WITH PRECISION CONTROLLED DELAY

June 6, 2006

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

INFORMATION DISCLOSURE STATEMENT

As suggested by 37 C.F.R. 1.97, the undersigned attorney brings to the attention of the Patent and Trademark Office the references listed on the attached form PTO/SB/08a. A copy of each listed foreign patent document and article is attached.

This is not to be construed as a representation that a search has been made or that no better prior art exists, or that a reference is relevant merely because cited.

The Examiner is requested to initial the attached form PTO/SB/08a and to return a copy of the initialed document to the undersigned as an indication that the attached references have been considered and made of record.

Respectfully submitted,

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JAPZOREC'C PCT/PTO 06 JUNTEDES 108a 'Sheet SERIAL NO. ATTY. DOCKET NO. INFORMATION DISCLOSURE Unknow 11581786 **CITATION** 3670-66 APPLICANT GEVORGIAN ET AL. FILING DATE TC/A.U. (Use several sheets if necessary) Unknown June 6, 2006 **U.S. PATENT DOCUMENTS** *EXAMINER **FILING DATE** SUBCLASS IF APPROPRIATE **CLASS** INITIAL **DOCUMENT NUMBER** DATE NAME 9/2000 Donnelly et al. 6,125,157 2/2002 6,350,335 Hampel et al. FOREIGN PATENT DOCUMENTS TRANSLATION **SUBCLASS** DOCUMENT DATE COUNTRY CLASS YES NO 99/43036 8/1999 WO ABST OTHER DOCUMENTS (including Author, Title, Date, Pertinent pages, etc.) International Search Report for PCT/SE2003/001918 dated 2 August 2004. Eto et al., A 333MHz, 20mW, 18ps resolution digital DLL using current-controlled delay with parallel variable resistor DAC (PVR-DAC), Proceedings of the Second IEEE Asia Pacific Conference on ASICS, 2000, pp. 349-350.

*Examiner Date Considered